

#2  
5-18-01

JC932 U.S. PTO  
09/677913  
10/03/00

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of: :  
: Gary S. Ditlow et al. : Atty Docket No.: BUR9-2000-0024-US1  
: :  
Serial No.: To be assigned : Art Unit: To be assigned  
: :  
Filed: Herewith : Examiner: To be assigned  
: :  
For: METHOD OF POWER DISTRIBUTION ANALYSIS FOR I/O CIRCUITS IN  
ASIC DESIGNS

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

In compliance with the Applicant's duty of disclosure under 37 CFR § 1.56, the undersigned hereby submits the documents listed on the attached Form PTO-1449 for consideration by the Examiner in charge of the above-identified patent application.

The submission shall not be construed as a representation that a search has been made or that no other art than that identified exists.

These documents are being submitted concurrently with the filing of the above application and it is, therefore, believed that no fee is due. However, the Commissioner is hereby authorized to charge payment of any deficiency in the above fee(s) or to charge

any additional fees required under 37 CFR § 1.16 or 1.17 or credit any overpayment to  
Deposit Account No. 22-0185.

Respectfully submitted,

A handwritten signature in cursive script, reading "William E. Curry".

William E. Curry, Reg.No. 43,572  
Pollock, Vande Sande & Amernick, R.L.L.P.  
1990 M Street, N.W.  
Washington, D.C. 20036-3425  
Telephone: 202-331-7111

Date: September 27, 2000